

## ***BLOCKX-SEMI PROFILE***

# MISSION

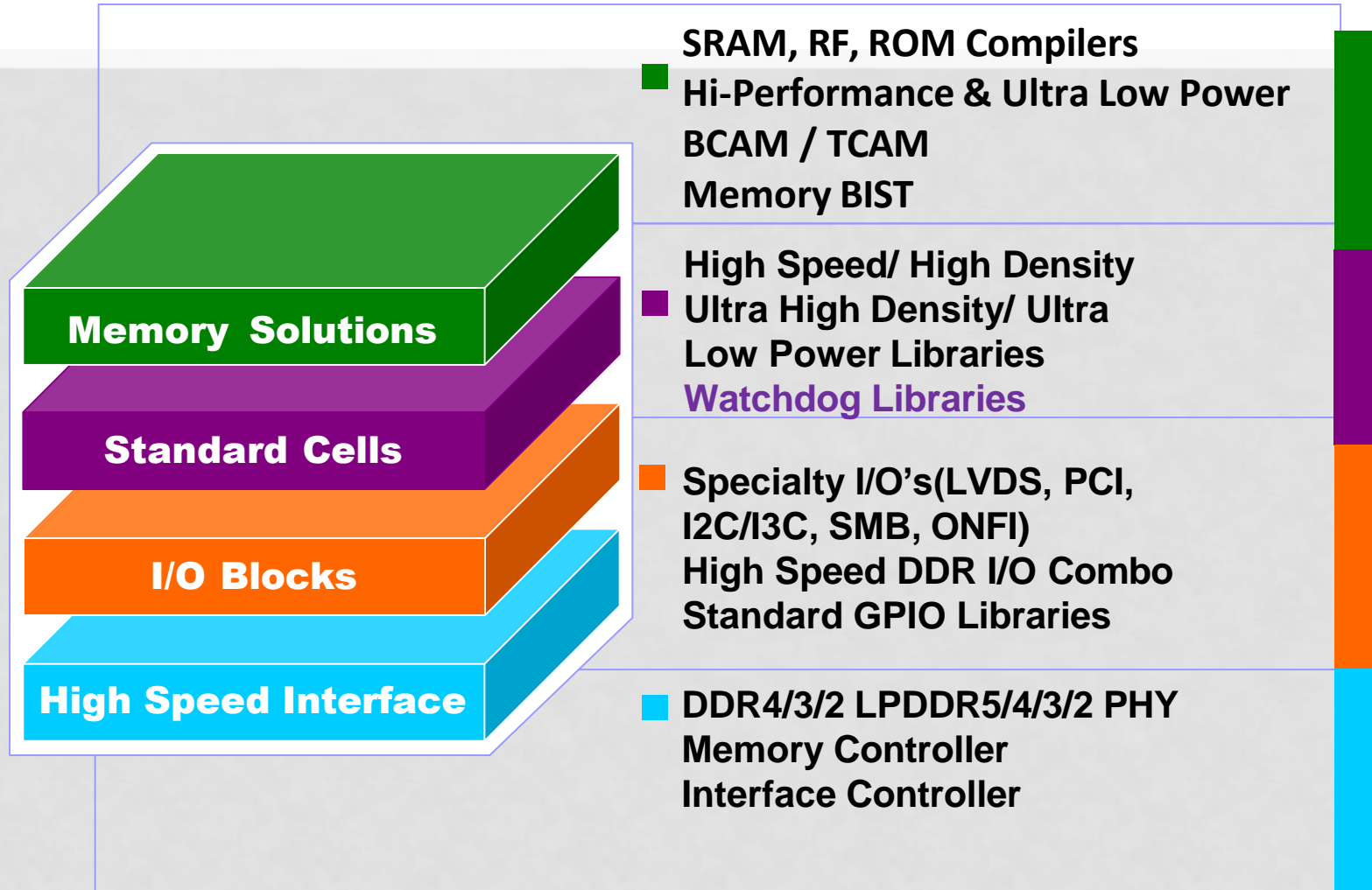
**BLOCKX-SEMI Technology is focused on providing Value added, high performance and low power, quality Semiconductor IP (SIP) to maximize the efficiency of hardware design teams. BLOCKX-SEMI is committed to:**

- 1. Provide a comprehensive high quality Semiconductor IP to satisfy most customer's needs and provide a one stop solution.**
- 2. Promptly respond to customer's design requests.**
- 3. Leverage on already silicon proven designs and various foundry process capabilities.**

# OUR CUSTOMERS



# PRODUCT OVERVIEW



# MEMORY PRODUCTS

- **Single and Dual Port SRAM** with both Row and Column redundancy with following Low Power options:
  - Low Leakage (light and deep sleep)
  - Power Gating with retention and without retention
  - Dual Rail (SRAM Periphery at lower Voltage)
  - Input Isolation
- **1-Port and 2-port Register File** with Column redundancy and all the above Low power options
- **Pseudo 2-Port Register Files** Compiler
- **Multi-Banking Single Port SRAM** compiler for larger SRAMs
- **ROM** Compiler
- **Memory BIST and Repair**

# MEMORY PROCESS NODES

- **3/5/6/7 FF/FF+**
- **12 FFC/FFC+**
- **16 FFC/FF+**
- **22 ULL/ULP**
- **28 HPCP/ULL/ULP**
- **40/55/65 LP/ULP/GP**
- **80/90 GP**

# STANDARD CELLS PRODUCTS

- **Up to 11000 cells**
- **Available in multiple channel lengths**
- **Thick-oxide Always-on, 1.8V and 2.5V**
- **Low Power Library Variant**
- **High Performance Library Variant**

# STANDARD CELLS PRODUCTS

	7+/7/ 6/5/3nm	12nm	16nm	28/ 22nm	40nm	65/ 55nm	90/ 80nm
6 track	☑	☑	☑		☑	☑	
6.5 track				☑			
7 track				☑	☑	☑	☑
7.5 track	☑		☑				
8 track	☑						
9 track	☑		☑	☑			
10 track				☑	☑	☑	☑
10.5 track			☑				
12 track			☑	☑	☑		
14 track				☑			

# 3NM STANDARD CELLS PRODUCTS

- **5.5 Track,** Ultra High Density, Low Power
- **6.5 Track,** Very High Density, Low Power

Libraries available in 2 poly pitches of 48 and 54nm



# 5/4NM STANDARD CELLS PRODUCTS

- **6 Track,**      Ultra High Density, Low Power
- **8 Track,**      Very High Density, Low Power

Libraries available in 2 poly pitches of 51 and 57nm

# I/O PRODUCTS

	7+/7/ 6/5/3nm	12nm	16nm	28/ 22nm	40nm	65/ 55nm	90/ 80nm
<b>GPIO</b>	☑	☑	☑	☑	☑	☑	☑
<b>DDR/LPDDR</b>	☑	☑	☑	☑	☑	☑	☑
<b>I<sup>2</sup>C/I<sup>3</sup>C, I<sup>2</sup>S</b>	☑	☑	☑	☑	☑	☑	☑
<b>LVDS</b>	☑	☑	☑	☑	☑	☑	☑
<b>CML</b>	☑	☑	☑	☑			☑
<b>LVPECL</b>	☑	☑	☑				☑
<b>eMMC</b>	☑	☑	☑	☑	☑	☑	
<b>ONFI</b>	☑	☑	☑	☑	☑		
<b>MDIO</b>	☑	☑	☑				
<b>RGMI</b>	☑	☑	☑	☑			
<b>Osc. Pad</b>	☑	☑	☑	☑	☑	☑	
<b>Multi Func.</b>				☑	☑	☑	☑

# 3NM IO PRODUCTS

- **GPIO 1.2v/1.8v Capable, Failsafe IO**
- **LPDDR4 IO**
- **I<sup>3</sup>C 1.2v/1.8v capable supporting different speeds**
- **LVDS**
- **Oscillator Pad (32K and 1-50MHz)**
- **DLL**

# 3NM IO PRODUCTS (UNDER DEVELOPMENT)

- **GPIO 1.2v/1.8v Tolerant**
- **DDR IO (A)** DDR5/4/3/3L and LPDDR4/3/2 Combo for 1.1/1.2/1.36/1.5v operation depend on standard (4266 Mbps)
- **DDR IO (B)** DDR5/DDR4 Combo IO (6400Mbps)
- **DDR IO (C)** LPDDR5/4x IO for 0.5v/0.6v operation (6400Mbps)
- **I<sup>2</sup>C 1.2v/1.8v** capable supporting different speeds
- **CML, LVPECL**
- **eMMC, ONFI 5, 4.2 ; MDIO, RGMII**

# 7/6, 5/4NM IO PRODUCTS

- **GPIO** 1.8v/3.0v (5nm: 1.65v max) **Tolerant, Failsafe IO**
- **GPIO** 1.2v/1.8v/2.5v/3.0v\* **Capable, Failsafe IO**
- \*7nm: 3.3v max, 5nm: 2.7v max (supporting 3.3v in progress)
- **DDR IO (A)** DDR5/4/3/3L and LPDDR4/3/2 Combo for 1.1/1.2/1.36/1.5v operation depend on standard (4266 Mbps)
- **DDR IO (B)** DDR5/DDR4 Combo IO (6400Mbps)
- **DDR IO (C)** LPDDR5/4x IO for 0.5v/0.6v operation (6400Mbps)
- **HSTL IO** 1.5v/1.8v
- **I<sup>2</sup>C/ I<sup>3</sup>C** 1.8v/3.3v capable supporting different speeds
- **LVDS , CML, LVPECL**

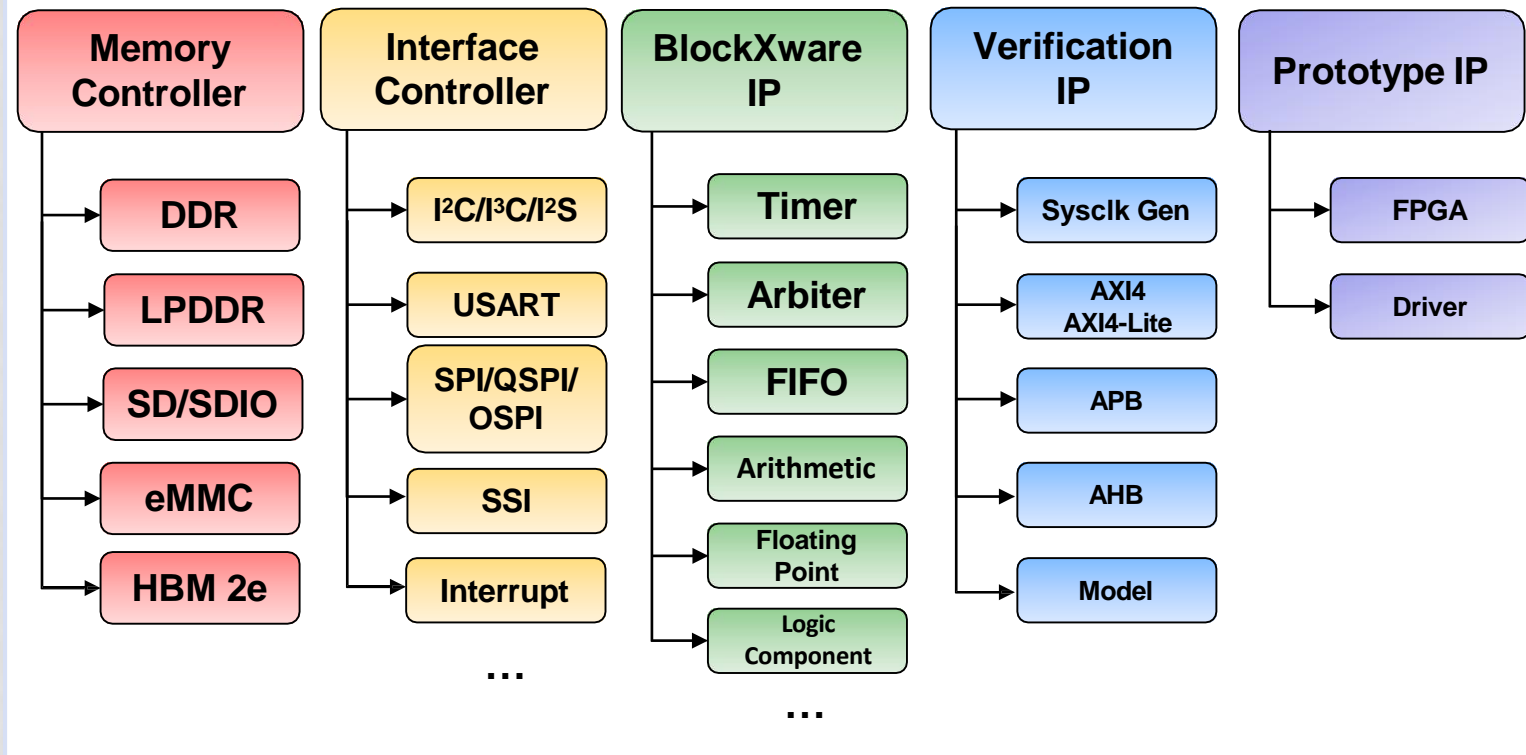
# DDR4/LPDDR4 PHY

- Fully configurable hardened DDR4/3/2, LPDDR5/4/3/2 PHY + DDR Controller Solution
- LPDDR4: Speed up to 4266Mbps
- LPDDR5: Speed up to 6400Mbps
- DFI 3.1/3.2/4.0 compliant
- Supports PHY independent read/write leveling & gate training
- Supports multi-rank, multi-gear ratio
- Built-in self testability
- Available in wire-bond and flip-chip versions
- Sideband and Inline ECC
- Compliance to automotive quality standard, fault coverage 99.8%

# SOFTWARE PRODUCTS

- **In-house EDA tool: Schematic, Layout, DRC/LVS**
- **Memory Compiler, IO Compiler**
- **Characterization flow, auto QA flow**
- **HDL Obfuscating, auto HDL generation**

# SOFT IP





# PRODUCTS LIST

**Memory Controller  
Storage Controller**

Peripheral Controller

BlockXware IP

Verification IP

- SDR Controller
- DDR4/3/2 Controller
- LPDDR4/3/2 Controller
- LPDDR5 Controller (On Going)
- eMMC Controller
- SD/SDIO Controller
- UHS-II Controller
- HBM 2e (On Going)
- PSRAM Controller
- ONFI Controller (On Going)
- DMA Controller (On Going)

# PRODUCTS LIST

Memory Controller  
Storage Controller

Peripheral Controller

BlockXware IP

Verification IP

- I<sup>2</sup>C, I<sup>2</sup>S Controller
- I<sup>3</sup>C Controller (On Going)
- UART/USART Controller
- SPI/QSPI/OSPI Controller
- SSI Controller
- Interrupt Controller
- JTAG Controller
- PVT Monitor
- GPIO Controller
- AXI4 Slave Interface
- APB Slave Interface
- AHB Slave Interface
- AXI4 Crossbar
- PWM Controller
- PDM2PCM, PCM2PDM
- Interface Bridge

# PRODUCTS LIST

Memory Controller  
Storage Controller

Peripheral Controller

**BlockXware IP**

Verification IP

- Data Integrity: encoder, decoder, ECC, CRC, AES, detector, parity...
- Arbiter
- Logic Component: counter, timer, registers, LFSR, multiplexer, DBI...
- FIFO
- Arithmetic Component: fixed and floating point adder, converter, multiplier, divider...

# PRODUCTS LIST

**Memory Controller  
Storage Controller**

**Peripheral Controller**

**BlockXware IP**

**Verification IP**

- APB verification IP
- AXI4 Master Bus-Functional-Model
- AXI4-Lite Master Bus-Functional-Model
- AXI4-Lite Verification IP
- AXI4 Verification IP
- AHB Verification IP
- Common Functions for Verification
- PCIe Verification IP
- Sequence manager
- System Clock Generator

# QUALIFICATION

- Experience in AMBA specifications: AXI4, AXI4-Lite, APB, AHB
- Experience in Peripheral Interfaces: I<sup>2</sup>C, I<sup>2</sup>S, I<sup>3</sup>C, USART, SPI,...
- Experience in JEDEC specifications: JESD229 (SDR), JESD79-4/3/2 (DDR), JESD209-5/4/3/2 (LPDDR), JESD235 (HBM), JESD84 (eMMC),...
- Experience in working with Synopsys, Mentor and Cadence Softwares for synthesis, simulation, DFT, Lint/CDC check, ...
- Experience in developing full test environment using UVM
- Experience in FPGA Prototypes: Intel Altera, AMD Xilinx

# BLOCKX-SEMI EXPERTISE

**Design Soft IP  
(FE & BE)**

**Verification Soft  
IP**

**Release Soft IP**

**Design  
Schematic Std-  
Cell**

**Layout Std-Cell**

**Characterize &  
Test Std-Cell**

**QA & Release  
Std-Cell**

**Design  
Schematic  
Memory**

**Layout Memory**

**Characterize &  
Test Memory**

**QA & Release  
Memory**

**Design  
Schematic I/O**

**Layout I/O**

**Characterize &  
Test I/O**

**QA & Release  
I/O**

# IC DESIGN SERVICES

- **Provides a wide range of ready silicon-IP**
- **Full turnkey custom digital circuit design and layout services**
- **Build cutting edge Design/Verification soft IPs and offer SoC/IP design/verification services**

***Thank you!***